AMENDMENTS TO THE CLAIMS

1. (Previously Presented) An array substrate for a liquid crystal display, the array substrate comprising:

a substrate;

a plurality of gate lines and a plurality of thin film transistors each having a gate electrode, a source electrode, a drain electrode and an active layer formed over the substrate;

an interlayer insulating layer formed on the thin film transistors;

a first gate redundancy line formed on the interlayer insulating layer, and connected electrically with just one of the gate electrodes, one of the gate lines, and both gate electrode and gate line through a first gate contact hole and formed of the same material as one of the source and drain electrodes;

a passivation layer provided on the first gate redundancy line and the interlayer insulating layer; and

a pixel electrode electrically connected with the drain electrode through the drain contact hole formed in the passivation layer.

2. (Original) The array substrate according to claim 1, wherein the thin film transistor is a top-gate thin film transistor.

3. (Original) The array substrate according to claim 2, wherein the first gate contact hole is formed passing through the interlayer insulating layer.

4. (Original) The array substrate according to claim 1, wherein the thin film transistor is a bottom-gate thin film transistor.

5. (Original) The array substrate according to claim 4, wherein the first gate contact hole is formed passing through the gate insulating layer and the interlayer insulating layer.

6. (Original) The array substrate according to claim 1, further comprising a second gate redundancy line formed on the passivation layer, and connected electrically with the first

gate redundancy line through a second gate contact hole and formed of the same material as the pixel electrode.

7. (Previously Presented) The array substrate according to claim 1, wherein the first gate redundancy line electrically connects with a gate line though a second gate contact hole.

8. (Previously Presented) An array substrate for a liquid crystal display, the array substrate comprising:

a substrate;

a plurality of gate lines and a plurality of thin film transistors each having a gate electrode, a source electrode, a drain electrode and an active layer formed on the substrate;

an interlayer insulating layer formed on the thin film transistors;

a passivation layer formed on the interlayer insulating layer;

a pixel electrode electrically connected with the drain electrode through a drain contact hole formed in the passivation layer; and

a gate redundancy line formed on the passivation layer, and connected electrically with just one of the gate electrodes, the gate lines, and both gate electrode and gate line through a gate contact hole and formed of the same material as the pixel electrode.

9. (Original) The array substrate according to claim 8, wherein the thin film transistor is a top-gate thin film transistor.

10. (Original) The array substrate according to claim 9, wherein the gate contact hole is formed passing through the interlayer insulating layer and passivation layer.

11. (Original) The array substrate according to claim 8, wherein the thin film transistor is a bottom-gate thin film transistor.

12. (Original) The array substrate according to claim 11, wherein the gate contact hole is formed passing through the gate insulating layer, the interlayer insulating layer, and the passivation layer.

13. (Previously Presented) The array substrate according to claim 8, wherein the gate redundancy line electrically connects with a gate line though a second gate contact hole.

14. (Previously Presented) A method of fabricating an array substrate for a liquid crystal display, the method comprising:

forming a plurality of gate lines and gate electrodes on a substrate;

forming an interlayer insulating layer on the gate lines and the gate electrodes;

forming a plurality of thin film transistors with the gate electrodes, source electrodes, drain electrodes, and active layers;

forming a first gate redundancy line on the interlayer insulating layer electrically connected with just one of the gate electrodes, the gate lines, and both the gate electrode and gate line through a first gate contact hole;

forming a passivation layer on the first gate redundancy line and the interlayer insulating layer; and

forming a drain contact hole in the passivation layer, and forming a pixel electrode connected electrically with the drain electrode through the drain contact hole.

15. (Original) The fabrication method according to claim 14, wherein the first gate redundancy line is formed with the same process and of the same material as one of the source electrode and drain electrode.

16. (Original) The fabrication method according to claim 14, wherein the thin film transistor having the gate electrode and the source electrode, and the drain electrode is formed in a top-gate manner.

17. (Original) The fabrication method according to claim 16, wherein the first gate contact hole is formed passing through the interlayer insulating layer.

18. (Original) The fabrication method according to claim 14, wherein thin film transistor having the gate electrode and the source electrode, and the drain electrode is formed in a bottom-gate manner.

19. (Original) The fabrication method according to claim 18, including forming a gate insulating layer between the gate electrode and the active layer, wherein the first gate contact hole is formed passing through the gate insulating layer and the interlayer insulating layer.

20. (Original) The fabrication method according to claim 14, further comprising forming a second gate redundancy line on the passivation layer connected electrically with the first gate redundancy line through a second gate contact hole.

21. (Original) The fabrication method according to claim 20, wherein the second gate redundancy line is formed in the same process and of the same material as the pixel electrode.

22. (Original) The fabrication method according to claim 20, wherein the second gate contact hole is formed passing through the passivation layer on the first gate redundancy line.

23. (Original) The fabrication method according to claim 14, further comprising forming a second gate contact hole wherein the first gate redundancy line electrically connects with the gate line though the second gate contact hole.

24. (Previously Presented) A method of fabricating an array substrate for a liquid crystal display, the method comprising:

forming a plurality of gate lines and gate electrodes on a substrate;

forming an interlayer insulating layer on the gate line and the gate electrode;

forming a plurality of thin film transistors with gate electrodes, source electrodes, drain electrodes, and active layers;

forming a passivation layer on the interlayer insulating layer and the thin film transistors; and

forming a gate contact hole in the passivation layer, and forming a gate redundancy line connected electrically with just one of the gate electrodes, the gate lines, and both gate electrode and gate line through the gate contact hole.

25. (Original) The fabrication method according to claim 24, wherein the gate redundancy line is formed with the same process and the same material as the pixel electrode.

26. (Original) The fabrication method according to claim 24, wherein the thin film transistor is formed in a top-gate manner.

27. (Original) The fabrication method according to claim 26, wherein the gate contact hole is formed passing through the interlayer insulating layer and passivation layer.

28. (Original) The fabrication method according to claim 24, wherein the thin film transistor is formed in a bottom-gate manner.

29. (Original) The fabrication method according to claim 28, including forming a gate insulating layer between the gate electrode and the active layer, wherein the gate contact hole is formed passing through the gate insulating layer, the interlayer insulating layer, gate insulating layer and the passivation layer.

30. (Original) The fabrication method according to claim 24, further comprising forming a second gate contact hole in the passivation layer and interlayer insulating layer wherein the gate redundancy line electrically connects with the gate line though a second gate contact hole.